UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,295	01/21/2004	Kenji Arai	031948-6	9845

22204 7590 03/20/2006

NIXON PEABODY, LLP
401 9TH STREET, NW
SUITE 900
WASHINGTON, DC 20004-2128

EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/760,295	ARAI ET AL.
	Examiner	Art Unit
	Helen Rossoshek	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-12,15-19* is/are rejected.

7)☒ Claim(s) *5,6,13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/760,295 filed 01/21/2004.

2. Claims 1-18 are pending in the Application.

Drawings

3. The drawings are objected to because: Fig. 3 does not have all labels of some elements, while they are in the description of the figure in the Specification (page 7).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 10, 11, 15-19 are objected to because of the following informalities: it is not clear what the Applicant intend to mean by "first one", "second one", third one" "fourth one".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Kitahara (US Patent 6,389,584).

With respect to claim 1 Kitahara teaches a method of laying out an integrated circuit having a semiconductor substrate and metal interconnecting lines disposed above the semiconductor substrate as shown on the Figs. 1a, 1b, 2a, 2b (col. 1, ll.39-46; col. 2, ll.38-44), the metal interconnecting lines including a core ring with a first power line and a first ground line, the first power line and the first ground line being mutually adjacent, the core ring supplying power to circuits surrounded by the core ring as shown on the as shown on the Figs. 2a-2c, 3a-3c, 5a-5c and 9, wherein, for example the Fig. 5a depicts integrated circuit layout typically including substrate, interconnecting lines disposed above semiconductor substrate, wherein metal interconnecting layers M1, M2, M3 include typically metal interconnecting lines including a core ring with a pair

of power and ground lines (Vdd and Vss) and core ring supplies the power from Signal source 558a (Fig. 5a) to the circuits surrounded by the core ring (Fig. 9) (col. 8, ll.8-18; col. 2, ll.38-44), the method comprising: laying out at least one metal-oxide-semiconductor (MOS) capacitor unit below the core ring the MOS capacitor unit having an active area disposed in the semiconductor substrate and an insulated gate electrode disposed on the semiconductor substrate, at least part of the insulated gate electrode being disposed above part of the active area as shown, for example, on the Figs. 3a-3c, wherein plurality MOS transistors Qp (MOS capacitor unit) (col. 1, ll.60-67) are laying out below the core ring (disposed on the metal layers M1-M3), wherein each MOS transistor has active area as source S and drain D areas and wherein insulated gate electrode G (Fig. 3a; col. 2, ll.16-21) and 26 (Fig. 2d) disposed on the semiconductor substrate and at least part of the insulated gate electrode is disposed above of the active area (drain and source), wherein the gate covers substantially the entire channel region (active area) (col. 1, ll.46-53); laying out first contacts connecting the active area to one of the first power line and the first ground line as shown on the Fig. 3c, wherein connecting active area (source and drain areas) of Qp and Qn with power line Vdd and ground line Vss (col. 1, ll.57-59), and; laying out second contacts connecting the insulated gate electrode to another one of the first power line and the first ground line as shown on the Fig. 3c, wherein the insulating gate electrode with power line and ground line (col. 2, ll.46-59).

With respect to claims 2-4 Kitahara teaches:

Claim 2: wherein the active area is disposed only below the first power line, the first contacts connecting the active area to the first power line, the second contacts connecting the insulated gate electrode to the first ground line as shown on the Fig. 5B active area of transistor Qp such as source S and drain D is disposed below the first power line located on the metal layer M2 (which is above of the transistor Qp) and connected to the first Vdd, and the insulated gate electrode G of the transistor Qp is connected to the first ground line Vss (col. 1, ll.56-58);

Claim 3: wherein the active area is disposed only below the first ground line, the first contacts connecting the active area to the first ground line, the second contacts connecting the insulated gate electrode to the first power line as shown on the Fig. 5A active area of transistor Qp such as S and D is disposed below the first ground line located on the metal line M2 (which is above of the transistor Qp) and connected to the ground line depending on which part of the area needs to be protected from plasma damage (col. 1, ll.56-58);

Claim 4: further comprising laying out a metal guard ring adjacent to the active area of said at least one MOS capacitor unit within inserting antenna diode next to active area of the MOS transistor (col. 3, ll.9-15) as shown on the Figs. 3A-3C (col. 33-38);

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 7, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitahara as applied to claim 1 above, and further in view of Lai et al. (US Patent Application Publication (US 2004/0195629).

With respect to claims 7, 8 and Kitahara teaches the limitations from which the claims depend. However Kitahara lacks specifics regarding I/O rings for supplying power to I/O circuits disposed outside the core ring. Lai et al. teaches :

Claim 7: the core ring is surrounded by an I/O ring for supplying power to I/O circuits disposed outside the core ring, the I/O ring including a second power line and a second ground line as shown on the Fig. 1, wherein typically I/O pad (ring) supplying the power to internal circuits 12, including a second power line an second ground line, the method further comprising: laying out at least one additional MOS capacitor unit beneath the core ring within inserting transistors 14 for discharging electrostatic charges (paragraph [0005]); and routing a pair of the metal interconnecting lines from said at

least one additional MOS capacitor unit to the I/O ring as shown on the Fig. 1 (paragraph [0040]);

Claim 8: wherein the core ring is surrounded by an I/O ring for supplying power to I/O circuits disposed outside the core ring, the I/O ring including a second power line and a second ground line as shown on the Fig. 1, wherein typically I/O pad (ring) supplying the power to internal circuits 12, including a second power line an second ground line, the method further comprising: laying out at least one additional MOS capacitor unit between the core ring and the I/O ring within inserting transistors 16 for discharging electrostatic charges (paragraphs [0005]); and routing a pair of the metal interconnecting lines from said at least one additional MOS capacitor unit to the I/O ring as shown on the Fig. 1 (paragraph [0040]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Lai et al. to teach the specifics subject matter Kitahara does not teach, because it discloses the various circuit designs in using ESD protection circuit for discharging electrostatic charges coupled to I/O pad (paragraph [0043], abstract).

9. Claims 9-12, 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitahara in view of Lai et al.

With respect to claim 9 Kitahara teaches limitations similar to the limitations of the claim 1, but lacks specifics regarding I/O rings for supplying power to I/O circuits disposed outside the core ring. Lai et al. teaches laying out an integrated circuit having a semiconductor substrate and metal interconnecting lines disposed above the semiconductor substrate, the metal interconnecting lines including a core ring with a first

power line and a first ground line and an input-output (I/O) ring with a second power line and a second ground line, the first power line and the first ground line being mutually adjacent, the second power line and the second ground line being mutually adjacent, the I/O ring and the core ring being mutually adjacent, the I/O ring surrounding the core ring, the core ring supplying power to circuits surrounded by the core ring, the I/O ring supplying power to I/O circuits disposed outside the core ring as shown on the Fig. 1, wherein typically I/O pad (ring) supplying the power to internal circuits 12, including a second power line an second ground line including inserting transistors 14, 16 for discharging electrostatic charges (paragraph [0005]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Lai et al. to teach the specifics subject matter Kitahara does not teach, because it discloses the various circuit designs in using ESD protection circuit for discharging electrostatic charges coupled to I/O pad (paragraph [0043], abstract).

With respect to claims 10-12, 15-19 Kitahara teaches:

Claim 10: wherein the contacts connect the active area of the first one of the MOS units to one of the first power line and the first ground line, and connect the insulated gate electrode of the first one of the MOS units to another one of the first power line and the first ground line as shown on the Fig. 5B active area of transistor Qp such as source S and drain D is disposed below the first power line located on the metal layer M2 (which is above of the transistor Qp) and connected to the first Vdd, and the insulated gate electrode G of the transistor Qp is connected to the first ground line Vss

(col. 1, ll.56-58), wherein plurality of MOS transistors Qp-Qn and plurality of power lines and ground lines are shown;

Claim 11: wherein the contacts connect the active area of the second one of the MOS units to one of the first power line and the first ground line, and also connect the active area of the second one of the MOS units to one of the second power line and the second ground line as shown on the Fig. 5A active area of transistor Qp such as S and D is disposed below the first ground line located on the metal line M2 (which is above of the transistor Qp) and connected to the ground line depending on which part of the area needs to be protected from plasma damage (col. 1, ll.56-58), including the variations of different connections shown on the Figs. 3A-33C, 5A-5C;

Claim 12: wherein the contacts also connect the insulated gate electrode of the second one of the MOS units to one of the first ground line and the second ground line as shown on the Fig. 3C;

Claim 15: wherein the contacts cause at least a third one of the MOS units to function as a MOS capacitor connected to the I/O ring within the variations of inserting transistors Qp-Qn into the integrated circuit as shown in the shown on the Figs. 3A-33C, 5A-5C;

Claim 16: wherein the contacts connect the active area of the third one of the MOS units to one of the second power line and the second ground line, and connect the insulated gate electrode of the third one of the MOS units to another one of the second power line and the second ground line within the variations of inserting transistors Qp-Qn into the integrated circuit as shown in the shown on the Figs. 3A-33C, 5A-5C;

Claim 17: counting a number of simultaneously switched outputs in the I/O circuits; counting a number of protection transistors already connected to the I/O circuits; connecting a first number of the MOS units, including the second one of the MOS units, to function as protection transistors; and connecting a second number of the MOS units, including the third one of the MOS units, to function as MOS capacitors connected to the I/O ring; and determining the first number and the second number from the number of simultaneously switched outputs in the I/O circuits and the number of protection transistors already connected to the I/O circuits within establishing a ratio for each interconnect to a gate of the MOS transistors, wherein the ratio relates to the physical characteristics of the gate and interconnect and expresses the relationship between the area of the gate and interconnect including calculating of the number of gates and their interconnections (col. 4, ll.11-17) and including calculating the ratio for each segment of an interconnect to a gate input that is not yet connected to a signal source (col. 8, ll.66,67; col. 9, ll.1-7);

Claim 18: wherein the contacts connect the active area of at least a fourth one of the MOS units to the first power line and the first ground line, the fourth one of the MOS units functioning as a protection transistor within searching and analyzing all segments for signal ant the particular layer as shown in the flow chart of the Fig. 6A and calculating the ratio between area of the wire segment and the total gates area for making a decision of inserting more number of diode antenna for protection gate input of the MOS transistors from plasma damage (col. 11, ll.8-29);

Claim 19: wherein the contacts connect the insulated gate electrode of the fourth one of the MOS units to the first ground line within iterations in the process of searching and analyzing all segments for signal ant the particular layer as shown in the flow chart of the Fig. 6A and calculating the ratio between area of the wire segment and the total gates area for making a decision of inserting more number of diode antenna for protection gate input of the MOS transistors from plasma damage (col. 11, ll.35-48). However Kitahara lacks specifics regarding I/O rings for supplying power to I/O circuits disposed outside the core ring. Lai et al. teaches connecting MOS transistors to I/O ring as shown as shown on the Fig. 1, wherein typically I/O pad (ring) supplying the power to internal circuits 12, including a second power line an second ground line including inserting transistors 14, 16 for discharging electrostatic charges (paragraph [0005]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Lai et al. to teach the specifics subject matter Kitahara does not teach, because it discloses the various circuit designs in using ESD protection circuit for discharging electrostatic charges coupled to I/O pad (paragraph [0043], abstract).

Allowable Subject Matter

10. Claims 5, 6, 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach identifying a part of the core ring crossed by comparatively few of the I/O signal lines; calculating an antenna ratio of the first power line; and calculating an antenna ratio of the first ground line; wherein laying out said second contacts includes

connecting the insulated gate electrode to the first power line if the antenna ratio of the first power line is greater than the antenna ratio of the first ground line; and connecting the insulated gate electrode to the first ground line if the antenna ratio of the first ground line is greater than the antenna ratio of the first power line as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

STACY A WHITMORE
PRIMARY EXAMINER